# EE 505

## Lecture 13

### String DACs Current Steering DACs

Review from Last Lecture
DAC Architectures



### Single Slope



Single-Slope DAC

# **DAC** Architectures



Single-Slope DAC

Can be viewed as a time-domain DAC where resolution headroom is very large

Benefits of Single-Slope ADC?

- No matching required
- Very simple structure
- Mostly Digital
- Very low DNL
- Very fine resolution possible
- No previous code dependence
- No binary to thermometer decoder

Limitations of Single-Slope ADC?

- Slow conversion rate
- Large C
- Leakage currents that will be temperature dependent
- Nonlinearity in C?
- Nonlinearity in I<sub>REF</sub>

# **DAC** Architectures



Provides DAC with positive and negative outputs

Term "dual slope" means something different here than what we see in "dual slope" ADCs







Previous code dependent glitches

Previous code dependent settling

Linear settling of DAC outputs do not affect linearity if all have same settling times (for both sampled outputs and overall transient response

Incomplete settling introduces nonlinearities in transient response and usually in settled response

Previous code dependent outputs or settling almost always introduces nonlinearities

Glitches can be many LSB in magnitude and are often previous-code dependent

Glitches in output at transition points do not introduce nonlinearities in settled outputs but may introduce distortion in continuous-time outputs



- □ Simple structure
- Inherently monotone
- □ Very low DNL
- Potential for being very fast
- Low Power Dissipation
- □ Widely Used Approach (with appropriate considerations)

### Challenges:

- Managing INL
- Matching (resistors, switches)
- Leakage currents
- Large number of devices for n large (2<sup>n</sup> or 2<sup>n+1</sup> lines)
- Decoder
- Routing thermometer/bubble clocks
- Transients during Boolean transitions
- Glitches
- Switch implementation
- The venin impedance facing  $V_{\text{OUT}}$  highly code dependent

Conceptual

(minor variant where  $V_{OUT}(0,...0) \neq 0$ )



Practical level shift

## Switch Implementation



Other switch structures (such as bootstrapped switch) used but not for basic string DACs

# Switch Assignment



Challenges:

## Switch Impedances





## **Switch Parasitics**



- $C_{BD}$  and  $C_{BS}$  can be significant and cause rise-fall times to be position dependent
- C<sub>GDOL</sub> can cause "kickback" or feed-forward
- C<sub>GS</sub> can slow turn-on and turn-off time of switch



Additional Challenges:

- Capacitance on V<sub>OUT</sub> can be large
  - larger for p-channel devices
  - even larger for TG switches
- Switch impedances position dependent
- Kickback from switches to R-string
- Capacitance on each node (though small) of Rstring from switch
- Thevenin impedance facing V<sub>OUT</sub> highly code dependent
- Gradient effects may cause nonlinearities since common-centroid layout may not be practical if n is large



#### Additional Challenges

- Delay in Decoder may be significant
- Delay in Decoder may be previous code and current code dependent
- Intermediate undesired Boolean outputs
   may occur
  - These may cause undesired opening and closing of switches
  - o Could momentarily short out taps on R-string
  - Could introduce transients on all nodes of R-string that are code and previous code dependent



Capacitive loading due to switches



- Uses matrix decoder as analog MUX (don't synthesize decoder)
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)

#### Challenges

- Still many signals to route
- Large capacitance on V<sub>OUT</sub> (over 2<sup>n+1</sup> diff caps)
- Multiple previous code dependencies cause output transition time to be quite unpredictable
- Considerable transients introduced on R-string



Parasitic Capacitances in Tree Decoder



### **Previous-Code Dependent Settling**

Assume all C's (except those on the R-string) initially with 0V Red denotes V<sub>3</sub>, black denotes 0V, Purple some other voltage



### **Previous-Code Dependent Settling**

Assume all C's (except those on the R-string) were initially at 0V Red denotes  $V_3$ , green denotes  $V_6$ , black denotes 0V, Purple some other voltage

Transition from <010> to <101>

White boxes show capacitors dependent upon previous code <010>



### **Previous-Code Dependent Settling**

- Assume all C's (except those on the R-string) were initially at OV
- Red denotes  $V_3$ , green denotes  $V_6$ , black denotes 0V, Purple some other voltage
- Some capacitors may retain values from a previous input for many clock cycles for some inputs resulting I previous-previous dependence of even longer



- Uses tree decoder as analog MUX
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)
- Dramatically reduces capacitance on output and switching capacitances

 $V_{\text{OUT}}$ 

### Challenges

- Still many signals to route
- Multiple previous code dependencies cause output transition time to be quite unpredictable



### **Tree-Decoder in Digital Domain**

Single transistor used at each marked intersection for PTLAND gates

Dramatic reduction in capacitive loading at output

Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

Will become more complicated if both p-channel and n-channel switches needed



# Stay Safe and Stay Healthy !

## End of Lecture 13